SENSING CIRCUITRY FOR READING AND VERIFYING THE CONTENTS OF ELECTRICALLY PROGRAMMABLE AND ERASABLE NON-VOLATILE MEMORY CELLS, USEFUL IN LOW SUPPLY-VOLTAGE TECHNOLOGIES

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BACKGROUND

Technical Field

[1] The present invention relates to sensing circuitry for reading and verifying the contents of electrically programmable and erasable non-volatile memory cells, useful in low-supply-voltage technologies.

[2] Specifically, the invention relates to sensing circuitry for reading and verifying the contents of electrically programmable and erasable non-volatile memory cells, said sensing circuitry comprising a sense amplifier having a first sensing-circuit portion connected to a cell to be read and a second reference-load-circuit portion connected to a reference generator.

[3] The invention relates, particularly but not exclusively, to circuitry for sensing the state of memory cells in embedded applications with low supply voltages, this description making reference to that field of application for convenience of illustration only.

Prior Art

[4] As is well known, semiconductor memories are organized in cell arrays set up as rows or wordlines and columns or bitlines.

[5] Each cell has essentially a floating-gate transistor, which also has drain and source terminals. The floating gate is formed on top of a semiconductor substrate and separated from the substrate by a thin layer of gate oxide. A control gate is coupled capacitively to the floating gate through a dielectric layer, and metal electrodes are